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TRANSMITTAL FORM <small>(to be used for all correspondence after initial filing)</small>	Application Number	09/517541
	Filing Date	2 March 2000
	First Named Inventor	Kia Silverbrook
	Art Unit	3628
	Examiner Name	Nga B Nguyen
	Attorney Docket Number	AUTH15US
Total Number of Pages in This Submission		

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input checked="" type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input type="checkbox"/> Other Enclosure(s) (please identify below):
Remarks: _____ Email: kia.silverbrook@silverbrookresearch.com Telephone: 61-2-9818 6633 Facsimile : 61-2-9555 7762		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name			
Signature			
Printed name	Kia Silverbrook, Simon Robert Walmsley		
Date	March 23, 2006	Reg. No.	

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In the United States Patent and Trademark Office

Serial Number: 09/517,541
Application. Filed: March 02, 2000
Applicant: Kia Silverbrook and Simon Robert Walmsley
Application Title: Shielding Manipulations of Secret Data
Examiner/GAU: NGA B Nguyen 3628
Dated: March 23, 2006
At: Balmain, NSW
Docket No. AUTH15US

REPLY

Commissioner for Patents
Washington, District of Columbia 20231

Dear Sir:

In response to the Examiner's further Office Action of February 3, 2006 in the present RCE application the Applicant submits the accompanying text book extracts and the below Remarks.

Regarding Response to Arguments/Amendment

In the Office Action, the Examiner submits that the Applicant has not submitted any rebuttal of the well known statements made by the Examiner in the previous and current Office Actions, but has merely requested references disclosing the well known limitations.

The following is a specific rebuttal of the Examiner's statement of what is purported to be well known in the art.

Typical CMOS circuit applications, in which it is ensured that both nMOS and pMOS transistors do not turn on at the same time, are high current output drivers (at output pads) to minimise the peak current taken from the power supply. Such high current output drivers are not useable to manipulate any type of data, let alone secret data as claimed in the claimed invention.

In designing CMOS circuits for manipulating data it is well known to make the circuits as simple as possible, by using the minimum number of transistors and minimum size transistors consistent with the speed requirements of the circuit. These circuits then allow both nMOS and pMOS transistors to turn on momentarily which risks the emission of a light pulse, making the CMOS structure a "flashing" CMOS structure, as described by the present inventors in the present application.

The accompanying extracted pages of "Principles of CMOS VLSI design" clearly show that it is well known that conventional CMOS logic (which is based on the CMOS inverter) has a region during a change of state where both nMOS and pMOS transistors are turned on, and therefore exhibit intermediate resistance.